Code No: V0423/R07

SET - 1

II B.Tech II Semester, Regular Examinations, Apr - 2011

SWITCHING THEORY AND LOGIC DESIGN

(Electronics and Communications Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions

All Questions carry equal marks

1. a) Convert $(AB6.13)_{16}$ into its octal equivalent and Convert $(675.42)_8$ into base-16 number. (8M)
   b) Convert the gray code number 10101111 into binary number and convert the decimal number 78.216 into BCD format. (8M)

2. a) Convert the given expressions into canonical SOP form
   i) f= AB + BC + CA (ii) f = A+ AB + ABC (8M)
   b) Simplify the following expressions using k-map
   i) $f(A,B,C,D) = \sum m(0,1,3,7,15) + \sum d(2,11,12)$
   ii) $f(A,B,C,D) = \pi M(0,2,6,8,12) + \pi d(3,4,7,10,14)$ (8M)

3. Find the minimal expression using tabulation method for the given function
   $F(A,B,C,D,E) = \sum m (1,2,12,13,15,17,18,19,20,21,23,24,25,27,29,31)$ (16M)

4. a) Design and draw the circuit diagram of BCD to binary code converter. (8M)
   b) Design and draw the circuit diagram of an octal to binary priority encoder. (8M)

5. a) Design and draw the circuit diagram of a BCD to Excess-3 code converter using PLA. (8M)
   b) Give the comparison between PROM, PAL and PLA with respect to various performance features. (8M)

6. a) Give and explain the realization of JK- flip flop using SR- flip flop. (8M)
   b) Design and draw the logic diagram for MOD-6 ripple counter. Give the design considerations. (8M)

Code No: V0423/R07

SET - 1

7. Determine the minimal state equivalent of the state table given below and find the minimum length sequence that distinguishes states A and F. (16M)

Present state	**Next State, Z**	
	X = 0	**X= 1**
A	E,0	C,0
B	C,0	A,0
C	B,0	B,0
D	G,0	A,0
E	F,1	B,0
F	E,0	D,0
G	D,0	G,0

8. The digital system to be designed consists of two registers R_1, R_2 and a flip flop, E. The system counts number of 1's in the number loaded into register R_1 and sets register R_2 that number. Draw the ASM chart and design the control logic using multiplexers. (16M)

Code No: V0423/R07

SET - 2

II B.Tech II Semester, Regular Examinations, Apr - 2011

SWITCHING THEORY AND LOGIC DESIGN

(Electronics and Communications Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions

All Questions carry equal marks

1. a) Represent $(-17)_{10}$ in
   i) Sign magnitude
   ii) 1's Compliment
   iii) 2's Compliment representation (8M)
   b) If the Hamming code sequence 1100110 is transmitted and due to error in one position it is received as 1110110. Locate the position of the error bit using parity checks and give the method for obtaining the correct sequence. (8M)

2. a) Prove the following expression using Boolean algebra and De-Morgan's theorems.
   barY barZ+ barW barX barZ + barW X Y barZ + WYbarZ = barZ (8M)
   b) Perform the realization of all basic logic gates using Universal gates. (8M)

3. a) Using k-map method determine SOP form of the following switching function.
   f(w,x,y,z) = ∑ m (0,1,4,5,6,7,9,11,15) + ∑ d (10,14) (8M)
   b) Simplify the logic function Y(A,B,C,D) = ∑ m (0,1,3,7,8,9,11,15) using Quine-McCluskey minimization technique. (8M)

4. a) Implement the following switching function
   f (A,B,C,D) = ∑ m (0,2,3,6,8,9,12,14) using the multiplexer. (8M)
   b) Design and draw the circuit diagram of a BCD to Excess-3 code converter. (8M)

5. a) Define the term 'memory'. Give the classification of memories and explain in brief. (8M)
   b) Design a combinational circuit using ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number. (8M)

6. a) Design and draw the logic diagram for 3- bit synchronous counter using JK- flip flop. (8M)
   b) Design and draw the circuit diagram of a sequence generator to generate the sequence …1101011…. (8M)

Code No: V0423/R07

SET - 2

7. What is the sequence detector? Design a 2-input 2-output detector which produces an output 1 every time the sequence 0101 is detected. Dive the design considerations in detail. (16M)

8. a) Design and draw the ASM diagram for an 8-bit serial 2's complimenter. (8M)
   b) Give the ASM representation of a Mealy model sequential circuit. (8M)

Code No: V0423/R07

SET - 3

II B.Tech II Semester, Regular Examinations, Apr - 2011

SWITCHING THEORY AND LOGIC DESIGN

(Electronics and Communications Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions

All Questions carry equal marks

---

1. a) Subtract 14 from 46 using the 8-bit 2's compliment and Add -75 to +26 using 8-bit 2's compliment. (8M)

   b) Derive a single error correcting code for an 11-bit group 01101110101. (8M)

2. a) Simplify the following expressions and implement the same with NAND gate circuits.

   i) F = A bar B + ABD + AB bar D + bar A bar C bar D + bar A B bar C

   ii) G = BD + BC bar D + A bar B bar C bar D (8M)

   b) Draw the logic diagram for the following function using only two input NOR gates

   F= a (b + c d) + b bar c. (8M)

3. Simplify the following expression using necessary minimization technique.

   f = ∑ m (0,1,2,8,9,15,17,21,24,25,27,31) (16M)

4. a) Draw and explain the logic diagrams of full adder and full subtractor with their truth tables. (8M)

   b) Design and draw the circuit diagrams of even and odd parity bit generators for 4-bit inputs. (8M)

5. a) Implement F1= bar A BC + A bar C + A barb C and F2= bar A bar B bar C + BC using PAL logic diagram. (8M)

   b) Implement the following Boolean functions with PLA.

   F1 (A, B, C) = ∑ m (0, 1, 2, 4)

   F2 (A, B, C) = ∑ m (0, 5, 6, 7) (8M)

Code No: V0423/R07

SET - 3

6. a) Convert the D- flip flop into a JK-flip flop. Draw and explain the logic diagram. (8M)

b) Design and draw the logic diagram of a synchronous 3 –bit up-down counter using JK-flip flop. (8M)

7. a) Draw the logic diagram of Mealy model and explain its operation. (8M)

b) Obtain the set of maximal compatibles for the state table given below using the Merger table method. (8M)

Present state	Next State, Output			
	00	01	11	10
A	B,-	D,-	-	C,-
B	F,-	I,-	-	-
C	-	-	G,-	H,-
D	B,-	A,-	F,-	E,-
E	-	-	-	F,-
F	A,0	-	B,-	-,1
G	E,1	B,-	-	-
H	E,-	-	-	A,0
I	E,-	C,-	-	-

8. Determine the transition table for the waveform generator given below.

Present state	Next state , output Input X1,X2			
	00	01	10	11
A	B,1	B.1	B,1	B,1
B	C,0	C,1	C,1	A,0
C	D,0	D,1	A,0	X
D	A,0	A,0	X	X

Present the ASM representation. (16M)

Code No: V0423/R07

SET - 4

II B.Tech II Semester, Regular Examinations, Apr - 2011

SWITCHING THEORY AND LOGIC DESIGN

(Electronics and Communications Engineering)

Time: 3 hours Max Marks: 80

Answer any FIVE Questions

All Questions carry equal marks

---

1. a) i) Subtract 649-387 using 9's complement method.
   ii) Convert the binary $(10101101)_2$ to its Gray code. (8M)
   b) A 7-bit Hamming code is received as 0101101. What is its correct code? Explain. (8M)

2. a) i) Simplify the expression Y= bar ((AB + bar C) (bar (A + B) + C))
   ii) Obtain the canonical product of sum expression of Y (A, B, C) = (A+ bar B) (B+C) (A+ bar C) (8M)
   b) Realize the universal gates with basic logic gates. Draw the relevant logic diagrams. (8M)

3. a) Simplify the following expressions using k-map for the 4 variables A, B, C and D.
   i) Y = m1+m3+m5+m7+m8+m9+m12+m13.
   ii) Y = π (0,1,4,5,6,8,9,12,13,14). (8M)
   b) Find the minimum sum of products for the following Boolean expression using Quine-McCluskey method.
   F (w, x, y, z) = ∑ (1, 3, 4, 5, 9, 10, 11) + ∑ d (6, 8) (8M)

4. a) Design and explain BCD to Decimal decoder and draw its logic diagram. (8M)
   b) Design and explain a 4-bit binary to gray code converter and draw the logic diagram. (8M)

5. a) Generate the following Boolean functions using PAL and draw its structure.
   Y0 = ABCD
   Y1 = bar A B bar C + bar ABC + AC + AB bar C
   Y2 = bar ABC bar D + bar ABCD + ABCD
   Y3 = bar A B bar CD +bar ABC bar D + bar ABCD + ABC bar D (8M)
   b) Define static and dynamic hazards. Design a static hazard free switching circuit. (8M)

Code No: V0423/R07

SET - 4

6. a) Realize T-flip flop using SR-flip flop and draw the relevant logic diagram. (8M)
   b) Design and explain a MOD-3 counter using JK-flip flop. (8M)

7. Design a sequence detector that produces an output 1 whenever the sequence 101101 is detected. Draw the relevant logic diagram and explain its function. (16M)

8. Design an odd parity generator assuming that inputs are arriving in strings of 3-bit with a single space between successive strings. Draw the logic required and explain its functionality. Give its ASM representation. (16M)